

Tpw

Atty. Dkt. No. 016891-0857

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Mitsusa TAKAHASHI
Title: METHOD FOR
MANUFACTURING THIN FILM
TRANSISTOR
Appl. No.: 10/617,170
Filing Date: 07/11/2003
Examiner: I.U. Anya
Art Unit: 2825

AMENDMENT TRANSMITTAL

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an amendment in the above-identified application.

☐ Small Entity status under 37 C.F.R. § 1.9 and § 1.27 has been established by a previous assertion of Small Entity status.

☐ Assertion of Small Entity status is enclosed.

☒ The fee required for additional claims is calculated below:

	Claims As Amended		Previously Paid For		Extra Claims Present		Rate		Additional Claims Fee
Total Claims:	6	-	20	=	0	x	\$18.00	=	\$0.00
Independent Claims:	1	-	3	=	0	x	\$86.00	=	\$0.00
First presentation of any Multiple Dependent Claims:							+	\$290.00	= \$0.00
CLAIMS FEE TOTAL								=	\$0.00

- ☐ Applicant hereby petitions for an extension of time under 37 C.F.R. §1.136(a) for the total number of months checked below:

<input type="checkbox"/> Extension for response filed within the first month:	\$110.00	\$0.00
<input type="checkbox"/> Extension for response filed within the second month:	\$420.00	\$0.00
<input type="checkbox"/> Extension for response filed within the third month:	\$950.00	\$0.00
<input type="checkbox"/> Extension for response filed within the fourth month:	\$1,480.00	\$0.00
<input type="checkbox"/> Extension for response filed within the fifth month:	\$2,010.00	\$0.00
EXTENSION FEE TOTAL:		\$0.00
<input type="checkbox"/> Statutory Disclaimer Fee under 37 C.F.R. 1.20(d):	\$110.00	\$0.00
CLAIMS, EXTENSION AND DISCLAIMER FEE TOTAL:		\$0.00
<input type="checkbox"/> Small Entity Fees Apply (subtract ½ of above):		\$0.00
TOTAL FEE:		\$0.00

- ☐ Please charge Deposit Account No. 19-0741 in the amount of \$0.00. A duplicate copy of this transmittal is enclosed.
- ☐ A check in the amount of \$0.00 is enclosed.
- ☒ The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.

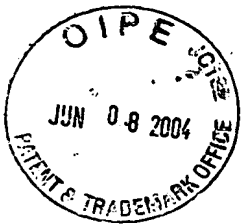
Respectfully submitted,

Date 3 June 2004

By Ronald Carlini 36,489

FOLEY & LARDNER LLP
Customer Number: 22428
Telephone: (202) 672-5407
Facsimile: (202) 672-5399

For David A. Blumenthal
Attorney for Applicant
Registration No. 26,257



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Mitsusa TAKAHASHI
Title: METHOD FOR MANUFACTURING
THIN FILM TRANSISTOR
Appl. No.: 10/617,170
Filing Date: July 11, 2003
Examiner: I. U. Anya
Art Unit: 2825

CERTIFICATE OF MAILING

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

I hereby certify that the following paper(s) and/or fee along with any attachments referred to or identified as being attached or enclosed are being deposited with the United States Postal Service as First Class Mail under 37 C.F.R. § 1.8(a) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450.

1. Amendment and Reply Under 37 CFR 1.111
2. Amendment Transmittal
3. Postcard

Respectfully submitted,

3 June 2004
Date

David A. Blumenthal
FOR David A. Blumenthal
Reg. No. 26,257

Foley & Lardner LLP
Customer Number: 22428
Telephone: (202) 672-5407
Facsimile: (202) 672-5399



Atty. Dkt. No. 016891-0857

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Mitsuasa TAKAHASHI
Title: METHOD FOR
MANUFACTURING THIN FILM
TRANSISTOR
Appl. No.: 10/617,170
Filing Date: 07/11/2003
Examiner: I.U. Anya
Art Unit: 2825

AMENDMENT AND REPLY UNDER 37 CFR 1.111

Mail Stop NON-FEE AMENDMENT
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

This communication is responsive to the Non-Final Office Action dated March 4, 2004, concerning the above-referenced patent application.

Please amend the application as follows:

In the Written Description:

Page 7, paragraph beginning at line 4, amend as follows:

An underlying oxide film 2 made of SiO₂ and having a thickness of about 300 nm is formed over a glass substrate 1 and an amorphous silicon film 3 is formed on the underlying oxide ~~film 3~~film 2 by LP-CVD or PE-CVD to have a thickness of about 60 nm. The amorphous silicon film 3 formed by PE-CVD is subjected to evacuation of hydrogen to allow the amorphous silicon film 3 to contain hydrogen not greater than 1 weight percent. Subsequently, a protection oxide film 4 of SiO₂ is formed on the amorphous silicon film 3 to have a thickness of about 50 nm and boron ions are implanted into the entire amorphous silicon film 3 at an energy of 50 keV and a dose of 7E12/cm² (FIG. 1A).

Page 8, paragraph beginning at line 12, amend as follows:

Under the aforementioned conditions, charged states in the spectrum of dangling bonds that occur at surfaces and interfaces in the amorphous silicon films within the N-channel transistor formation region and the P-channel transistor formation ~~region~~region 7 become nearly equal. Therefore, an advantageous mechanism that allows doped amorphous silicon to grow by solid phase at a higher rate can be observed. As a result, localized levels caused by dangling bonds that occur at surfaces and interfaces in the amorphous silicon film 3 are reduced to allow standard deviation (σ) of variations in threshold voltages of N-channel and P-channel transistors to be reduced to approximately half the standard deviation (σ) of variations in threshold voltages of N-channel and P-channel transistors formed in accordance with the conventional technique, i. e., reduced from 0.18 V to 0.11 V and from 0.25 V to 0.14 V, respectively.